



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/701,328

11/03/2003

Ernest Allen III

03-1781/LSIIP237

4927

24319

7590

02/11/2005

LSI LOGIC CORPORATION

1621 BARBER LANE

MS: D-106

MILPITAS, CA 95035

EXAMINER

DANG, PHUC T

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 02/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No. 10/701,328	Applicant(s) ALLEN ET AL.	
	Examiner PHUC T. DANG	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 November 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 9-14 is/are allowed.
- 6) ☒ Claim(s) 1,3 and 4 is/are rejected.
- 7) ☒ Claim(s) 2 and 5-8 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>110303</u> . | 6) <input type="checkbox"/> Other: _____ |

Art Unit: 2818

DETAILED ACTION

Election/Restrictions

1. Applicant's request filed on January 18, 2005 for reconsideration of the last Election/Restriction is persuasive, and, therefore, the Restriction filed on December 21, 2004 is withdrawn.
2. Claims 1-20 are currently still pending in the application.

Oath/Declaration

3. The oath/declaration filed on November 3, 2003 is acceptable.

Information Disclosure Statement

4. The office acknowledges receipt of the following items from the applicant:
Information Disclosure Statement (IDS) filed on November 3, 2003.

Specification

5. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2818

6. Claims 1 and 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gross (U.S. Patent No. 5,206,181) in view of McClure (U.S. Patent No. 5,557,573).

Gross discloses a method for manufacturing a semiconductor integrated circuit, the method comprising:

providing a wafer (10, Fig. 1) having a plurality of integrated circuit dies (12, Fig. 1);
using a test fixture (14, Figs. 1-2) to provide electrical contact with electrical testing structures located in a scribe line (13, Figs. 1-2)) adjacent to a first of the plurality of integrated circuit dies (12, Figs. 1-2).

Gross discloses all the features of the claimed invention as discussed above, but does not disclose monitoring the output of an identification cell located within the first of the plurality of integrated circuit dies by using the test fixture to provide contact with contacts on the wafer corresponding to the identification cell.

McClure, however, discloses a step of monitoring the output of an identification cell located within the first of the plurality of integrated circuit dies by using the test fixture to provide contact with contacts on the wafer corresponding to the identification cell [col. 7, lines 3-39].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teaching of McClure to Gross discussed above such that a step of monitoring the output of an identification cell located within the first of the plurality of integrated circuit dies by using the test fixture to provide contact with contacts on the wafer corresponding to the identification cell for a purpose of minimizing the number of signals used to control the integrated circuit during testing the wafer.

Art Unit: 2818

Regarding claim 3, Gross discloses the contacts are metallic pads [col. 6, lines 9-12].

Regarding claim 4, Gross discloses further comprising using the test fixture to access a contact on at least one of the plurality of integrated circuit dies to measure a performance parameter [col. 3, lines 45-49].

Allowable Subject Matter

7. Claims 9-20 would be allowed.

The following is a statement of reason for the indication of allowable subject matter:

Claims 9-20 are considered allowable since the prior art of record and the considered pertinent to the applicant's disclosure does not teach or suggest the claimed invention having an integrated circuit test fixture configured for interconnection between a semiconductor tester and a wafer, comprising a plurality of probe tips configured to provide electrical contact with a corresponding plurality of pads on a semiconductor wafer, wherein a first group of the plurality of pads comprises pads connected to an identification cell located within an integrated circuit die on the wafer and a second group of the plurality of pads is connected to an electrical testing structure located in a scribe line adjacent to the die as cited in claim 9 and monitoring the identification number before separating the plurality of dies from the wafer by using a generic interface configured to access pads on a plurality of different integrated circuit designs as cited in claim 14.

Claims 2 and 5-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

Art Unit: 2818

None of the Prior Art made of record discloses wherein the contacts are electrically connected to the identification cell and positioned in a predetermined standardized geometric location relative to the electrical testing structures located in the scribe line as cited in claim 2 and wherein the performance parameter is one of a supply current and a supply voltage as cited in claim 5 and wherein the performance parameter is a quiescent current as cited in claim 6 and wherein the output of an identification cell provides a unique identification number for the cell and further comprising storing the identification number along with location data indicating the location of the first of the plurality of integrated circuit dies on the wafer as cited in claim 7 and further comprising using the identification number and the location data in a post processing step to identify defects in the plurality of dies as cited in claim 8.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is (571) 272-1776. The examiner can normally be reached on 8:00 am-5:00 pm.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and After Final communications.

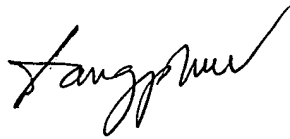
10. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Art Unit: 2818

Phuc T. Dang ^{PD}

Primary Examiner

Art Unit 2818

A handwritten signature in black ink, appearing to read "Phuc T. Dang", written in a cursive style.